**EENG 5560**

**ASSIGNMENT 1**

**Assigned – Jan 26, 2023**

**Due – Feb 2, 2023**

D

C

B

A

ADD, SUBTRACT, MULTIPLY

AND, OR, NAND, NOR, XOR, XNOR

GT, LT, EQ, GTE, LTE, Not EQ

G

* Use Xilinx Vivado to design and simulate the logic shown above.
* Inputs A, B, C, D are 8-bit wide.
* Make sure you test your design for all the operations listed above.

Submit vhdl code, RTL schematic, screenshots of simulation waveforms, , and test bench of the design. Test your design using at least five test cases. Mark two of the test cases and show the corresponding inputs, expected outputs and simulated outputs for those two cases. The source files should contain appropriate comments for better understanding.